



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,419	09/30/2003	Chih-Wei Hung	LKSP0020USA	2418
27765	7590	02/17/2005	EXAMINER	
NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)			HUYNH, ANDY	
P.O. BOX 506			ART UNIT	PAPER NUMBER
MERRIFIELD, VA 22116			2818	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Ak

**Office Action Summary**

Application No.

10/605,419

Applicant(s)

HUNG ET AL.

Examiner

Andy Huynh

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 January 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

In the Response to Restriction Requirement dated January 28, 2005, Applicant has elected Invention I, claims 1-9, drawn to a device and canceled claims 10-16 is acknowledged. Accordingly, claims 1-9 are currently pending in this application.

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in TAIWAN, 092101900 on 01/28/2003.

### ***Drawings***

The drawings are objected for the following reason.

Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6,091,644 hereinafter referred to as "Hsu") in view of Fan et al. (USP 6,747,310 hereinafter referred to as "Fan").

Regarding claim 1, Hsu discloses in Fig. 2A and corresponding texts as set forth in column 3, lines 30-62, a flash memory cell structure 200 comprises:

- a substrate 20 having a stacked gate G;
- a first-type doped region 25 located in the substrate as a drain;
- a shallow second-type doped region 26 located underneath the stacked gate and adjacent to the first-type doped region;
- a deep second-type doped region 27 surrounding the first-type doped region and adjacent to the shallow second-type doped region; and
- a doped source region formed on a side of the shallow second-type doped region as a source.

Hsu fails to teach a flash memory cell structure comprises a select gate formed on the substrate and adjacent to one side of the stacked gate. Fan teaches in Fig. 1 a flash memory cell comprises a select gate 18 formed on the substrate and adjacent to one side of the stacked gate. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of a flash memory cell comprising a select gate formed on the substrate and adjacent to one side of the stacked gate, as taught by Fan to incorporate into and modify the Hsu's structure to arrive the claimed limitation in order to achieve a memory cell is

Art Unit: 2818

very small in size and provide significantly enhanced programming and erase performance (col. 1, line 65-col. 2, line 2).

Regarding claim 2, Hsu discloses in Fig. 2A a depth of the deep second-type doped region is deeper than a depth of the shallow second-type doped region.

Regarding claim 3, Hsu discloses the deep second-type doped region has the same p-doped ions as the shallow second-type doped region.

Regarding claims 4 and 5, Hsu discloses the doped ions of the deep second-type doped region and the shallow second-type doped region are selected from the III A group, and the doped ions of the first-type doped region and the doped source region are selected from the V A group (col. 6, lines 57-64).

Regarding claims 6-8, Hsu discloses in Figs. 3A-3B the first-type doped region and the deep second-type doped region are electrically short-circuited together, the first-type doped region and the deep second-type doped region are electrically short-circuited by metal 30 penetrating the junction between the first-type doped region and the deep second-type doped region, and the first-type doped region and the deep second-type doped region are electrically short-circuited by metal 30 exposed outside the first-type doped region and the deep second-type doped region of the substrate.

Regarding claim 9, Hsu discloses in Fig. 2A the stacked gate includes a floating gate 24 located over the shallow second-type doped region, and a control gate 23 located over the floating gate.

Art Unit: 2818

*Conclusion*

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

02/16/05



Andy Huynh

Patent Examiner